METHOD FOR TESTING CHIPS ON FLAT SOLDER BUMPS

Abstract of the Disclosure

A method for testing integrated circuit chips with probe wires on flat solder bumps and IC chips that are equipped with flat solder bumps are disclosed. In the method, an IC chip that has a multiplicity of bond pads and a multiplicity of flat solder bumps are first provided in which each of the solder bumps has a height less than ½ of its diameter on the multiplicity of bond pads. The probe wires can thus be easily used to contact the increased target area on the solder bumps for establishing electrical connection with a test circuit. The probe can further be conducted easily with all the Z height of the bumps are substantially equal. The height of the solder bumps may be suitably controlled by either a planarization process in which soft solder bumps are compressed by a planar surface, or solder bumps are formed in an in-situ mold by either a MSS or an electroplating process for forming solder bumps in the shape of short cylinders. When the MSS method is used for planting the bumps, solder bumps are transferred onto the wafer surface in a substantially flattened hemi-spherical shape.